



FIG. 4

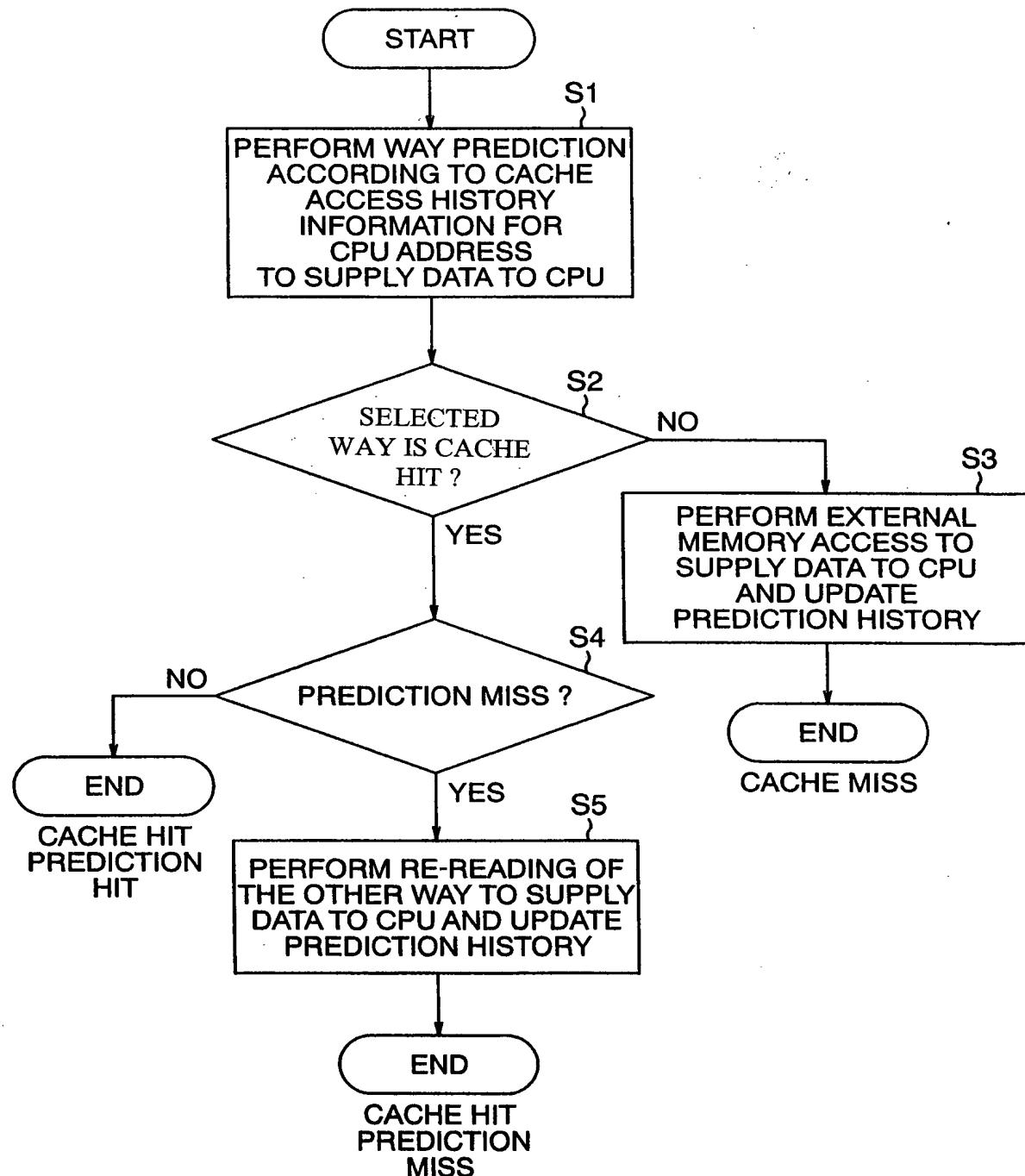


FIG. 5

FIG. 6

TIME	1	2	3	4	5	6	7	8	9	10	11	12	13	14
CLOCK														
CPU ADDRESS	R1	R2	R2	R2	R3	R4	R4	R4	R5					
ADDRESS ARRAY ACCESS	R1	(R2)		(R2)	R3	R4		(R4)	R5					
DATA ARRAY ACCESS	R1		R1	R2	R3		R3	R4	R5					
HISTORY INFORMATION PREDICTED WAY	W0	W0	W1	W0	W0	W0	W1	W0	W0					
WAY SELECTED	W0		W1	W1	W0		W1	W1	W0					
LOCATION OF CPU REQUESTING DATA	W1 for R1			W1 for R2	W1 for R3				W1 for R4	W1 for R5				
CPU RECEIVING DATA	W0 for R1		W1 for R1	W1 for R2	W0 for R3		W1 for R3	W1 for R4	W0 for R5					
ACCESS STATE	R1 IS PRE-DICTION MISS			R2 IS PRE-DICTION HIT	R3 IS PRE-DICTION MISS				R4 IS PRE-DICTION HIT	R5 IS PRE-DICTION MISS				
EXTERNAL MEMORY ACCESS														
COMPLETION SIGNAL	1	0	0	1	1	0	0	1	1					

Replacement sheet

FIG. 7

TIME	1	2	3	4	5	6	7	8	9	10	11	12	13	14
CLOCK														
CPU ADDRESS	R1	R2	R2	R2	R2	R2	R3	R3	R4	R4	R4	R4	R5	
ADDRESS ARRAY ACCESS	R1					R2			R3				R4	
DATA ARRAY ACCESS	R1					R2		R2	R3				R4	
HISTORY INFORMATION PREDICTED WAY	W0					W0		W1	W0				W0	
WAY SELECTED	W0					W0		W1	W0				W0	
LOCATION OF CPU REQUESTING DATA	EX- TERNAL MEMORY					W1 for R2			EX- TERNAL MEMORY				W1 for R2	
CPU RECEIVING DATA	W0 for R1				Data for R1	W0 for R2		W1 for R2	W0 for R3				Data for R3	W0 for R4
ACCESS STATE	R1 IS CACHE MISS					R2 IS PRE- DICTION MISS			R3 IS CACHE MISS				R4 IS PRE- DICTION MISS	
EXTERNAL MEMORY ACCESS	ISSUE R1								ISSUE R3					

FIG. 8

TIME	1	2	3	4	5	6	7	8	9	10	11	12	13	14
CLOCK														
CPU ADDRESS	R1	R2	R2	R2	R2	R2	R3	R4	R4	R4	R4	R4		
ADDRESS ARRAY ACCESS	R1	R2					(R2)	R3	R4				(R4)	
DATA ARRAY ACCESS	R1						R2	R3					R4	
HISTORY INFORMATION PREDICTED WAY	W0						W0	W0					W0	
WAY SELECTED	W0						W1	W0					W1	
LOCATION OF CPU REQUESTING DATA	EXTERNAL MEMORY						W1 for R2	EXTERNAL MEMORY					W1 for R4	
CPU RECEIVING DATA	W0 for R1				Data for R1	W1 for R2	W0 for R3					Data for R1	W1 for R4	
ACCESS STATE	R1 IS CACHE MISS					R2 IS PREDICTION HIT	R3 IS CACHE MISS						R4 IS PREDICTION HIT	
EXTERNAL MEMORY ACCESS		ISSUE R1						ISSUE R3						
COMPLETION SIGNAL	1	0	0	0	0	1	1	0	0	0	0	1	1	
		*						*						

FIG. 9

TIME	1	2	3	4	5	6	7	8	9	10	11	12	13	14
CLOCK														
CPU ADDRESS	R1	R2	R2	R2	R3	R3	R3	R3	R3	R4	R4	R4	R5	R5
ADDRESS ARRAY ACCESS	R1			R2					R3			R4		
DATA ARRAY ACCESS	R1		R1	R2					R3	R3	R3	R4		
HISTORY INFORMATION PREDICTED WAY	W0		W1	W0					W0	W1	W0			
WAY SELECTED	W0		W1	W0					W0	W1	W0			
LOCATION OF CPU REQUESTING DATA	W1 for R1			EX- TERNA L MEMO RY					W1 for R3			EX- TERNA L MEMO RY		
CPU RECEIVING DATA	W0 for R1		W1 for R1	W0 for R2				Data for R2	W0 for R3		W1 for R3	W0 for R4		
ACCESS STATE	R1 IS PRE- DICTION MISS			R2 IS CACHE MISS					R3 IS PRE- DICTION MISS			R4 IS CACHE MISS		
EXTERNAL MEMORY ACCESS					ISSUE R2							ISSUE R4		

Replacement sheet

FIG. 10

TIME	1	2	3	4	5	6	7	8	9	10	11	12	13	14
CLOCK														
CPU ADDRESS	R1	R2	R2	R2	R3	R3	R3	R4	R4	R4	R5	R5	R5	
ADDRESS ARRAY ACCESS	R1	R2		R2		R3	R4		R4		R5			
DATA ARRAY ACCESS	R1		R1	R2		R3		R3	R4		R5			
HISTORY INFORMATION PREDICTED WAY	W0		W1	W0		W0		W1	W0					
WAY SELECTED	W0		W1	W0		W0		W1	W0					
LOCATION OF CPU REQUESTING DATA	W1 for R1			EX- TERNA L MEMO RY			W1 for R3			EX- TERNA L MEMO RY				
CPU RECEIVING DATA	W0 for R1		W1 for R1	W0 for R1		Data for R2	W0 for R3		W1 for R1	W0 for R4		Data for R4		
ACCESS STATE	R1 IS PRE- DICTION MISS			R2 IS CACHE MISS			R3 IS PRE- DICTION MISS			R4 IS CACHE MISS				
EXTERNAL MEMORY ACCESS			ISSUE R2						ISSUE R4					
COMPLETION SIGNAL	1	0	0	1	0	0	1	0	0	1	0	0	1	